REMARKS

Please consider the following comments. Following this response, claims 1, 2, 4-16, and 26-43 are pending. Applicant respectfully requests reconsideration and allowance of this application in view of the above amendments and the following remarks.

Examiner Interview

Applicant wishes to again thank the Examiner for the telephonic interview of 6 December 2007. This response reflects the comments made by the undersigned during that interview.

Claim Rejections – 35 U.S.C. § 103

The Examiner has rejected claims 1, 5, 7, 26, and 27 under 35 U.S.C. § 103(a) as being allegedly unpatentable over United States Patent No. 6,469,345 to Aoki et al. ("Aoki") in view of United States Patent No. 6,465,325 to Ridley et al. ("Ridley") and in view of United States Published Patent Application No. 2001/0009304 to Tottori ("Tottori"). Applicant respectfully traverses this rejection.

However, in an effort to expedite prosecution, and in no way acquiescing to this rejection, Applicant has amended claim 1 to recite forming an interlayer over the conductive film, and that the annealing of the substrate is performed prior to forming the interlayer. Support for this comes, for example from paragraphs [0063], [0064], and [0078], and through the source region 8, body region 9, and interlayer insulation film 10 in Applicant's specification and drawings. Since the interlayer 10 is formed after forming the source region 8 and the body region 9 are formed, and the source region 8 and the body region 9 are formed after the annealing, the interlayer insulation film 10 must be formed after the annealing.

The Examiner cites Aoki as allegedly showing the operation of forming a trench through its formation of a trench 6, the operation of forming an insulation film in its formation of the silicon-oxide film 7a, and the operation of forming a conductive film through its forming a gate electrode 8. (See, e.g., Aoki, column 2, line 48, through column 4, linc 33, and FIG. 1, 2B, 2C, and 2G.) However, the Examiner acknowledges that Aoki fails to disclose annealing a substrate at an annealing temperature after the forming of the conductive film. For this teaching he relies upon a combination of Ridley and Tottori. Howevcr, a careful examination of Ridley and Tottori will show that they do not disclose or suggest both forming an interlayer over the conductive film, and that the annealing of the substrate is performed prior to forming the interlayer, as recited in claim 1.

Ridley discloses that following removal of a semiconductor material from an upper portion of the trench, an insulating barrier layer is formed on the sidewalls of the upper portion. The insulating barrier layer is preferably formed from low temperature oxide, silicon nitride, or silicon oxynitride. Two successive layers of BPSG are applied, one on top of the other. After the first layer of BPSG is applied, the temperature is raised above the conventional temperature of about 850°C, preferably about 1050°C, to a maximum of about 1100°C. (See, e.g., Ridley, column 3, lines 22-35, column 4, lines 44-49, and FIG. 6.) The Examiner then cites Tottori for a suggestion that the temperature of the annealing could rise to 1150°C. (See, e.g., Tottori, paragraph [0016].)

But in Ridley, the annealing is formed after a BPSG layer 44 is formed over a trench 40, and the annealing is performed for purposes of planarization. Nothing in Ridley discloses or suggests that the annealing be done *before* the formation of the BPSG layer 44. In fact, since the whole purpose of the annealing process is to planarize the BPSG layer 44, it would be contrary to

the teachings of Ridley to perform the annealing (i.e., the planarization operation) before the formation of the very layer that is to be annealed (i.e., planarized).

Tottori is only relied upon for a teaching of annealing using a higher temperature. Nothing in its teachings cure the deficiencies in Ridley noted above.

Therefore, for at least the reasons given above, nothing in Aoki, Ridley, or Tottori, alone or in combination, discloses or suggests all of the features recited in amended claim 1.

Claims 5, 7, 26, and 27 all ultimately depend from claim 1 and are allowable for at least the reasons given above for claim 1.

Therefore, for at least the reasons given above, Applicant respectfully requests that the Examiner withdraw the rejection of claims 1, 5, 7, 26, and 27 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Aoki in view of Ridley, and Tottori.

The Examiner has rejected claims 2, 4, 6, 8-11, 13, and 14 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Aoki, Ridley, and Tottori, and further in view of United States Patent No. 6,455,378 to Inagawa et al. ("Inagawa"). In addition, although not mentioned in the opening paragraph of this rejection, the Examiner has provided comments regarding claims 29 and 30 in the body of the rejection. Therefore, Applicant believes that this rejection was intended to cover claims 29 and 30. Applicant respectfully traverses this rejection.

However, in an effort to expedite prosecution, and in no way acquiescing to this rejection, Applicant has amended claim 11 to recite that the annealing is performed prior to performing the thermal diffusion process. Support for this comes, for example from paragraphs [0063], [0064], and [0078], and through the source region 8, body region 9 in Applicant's specification and drawings.

The Examiner cites Aoki as allegedly showing the operation of forming a trench through its formation of a trench 6, the operation of forming an insulation film in its formation of the silicon-oxide film 7a, the operation of forming a conductive film through its forming a gate electrode 8, and the operation of forming a source region through its formation of an N^+ type layer 4. (See, e.g., Aoki, column 2, line 48, through column 4, line 33, and FIG. 1, 2B, 2C, and 2G.) However, the Examiner acknowledges that Aoki fails to disclose annealing a substrate at an annealing temperature after the forming of the conductive film. For this teaching he relies upon a combination of Ridley and Tottori. However, a careful examination of Ridley and Tottori will show that they do not disclose or suggest that annealing is performed prior to performing the thermal diffusion process, as recited in claim 11.

Ridley discloses that following removal of a semiconductor material from an upper portion of the trench, an insulating barrier layer is formed on the sidewalls of the upper portion. The insulating barrier layer is preferably formed from low temperature oxide, silicon nitride, or silicon oxynitride. Two successive layers of BPSG are applied, one on top of the other. After the first layer of BPSG is applied, the temperature is raised above the conventional temperature of about 850°C, preferably about 1050°C, to a maximum of about 1100°C. (See, e.g., Ridley, column 3, lines 22-35, column 4, lines 44-49, and FIG. 6.) The Examiner then cites Tottori for a suggestion that the temperature of the annealing could rise to 1150°C. (See, e.g., Tottori, paragraph [0016].)

But in Ridley, the annealing is formed after a BPSG layer 44 is formed over a trench 40, and the annealing is performed for purposes of planarization. Nothing in Ridley discloses or suggests that the annealing be done *before* the formation of the BPSG layer 44. In fact, since the whole purpose of the annealing process is to planarize the BPSG layer 44, it would be contrary to the teachings of Ridley to perform the annealing (i.e., the planarization operation) before the

formation of the very layer that is to be annealed (i.e., planarized). And since the BPSG layer 44 in Ridley is formed over the source region 28, the annealing process must also take place after any thermal diffusion process that forms a source region. Thus, nothing in Ridley discloses or suggests that the annealing be done *before* a thermal diffusion process that forms a source region.

The Examiner relies upon Tottori only for a teaching of annealing using a higher temperature. Nothing in its teachings cure the deficiencies in Aoki and Ridley noted above. The Examiner relies upon Inagawa for a teaching that the gate electrode include a canopy. Nothing in Inagawa cures the deficiencies in Aoki, Ridley, and Tottori noted above.

Claims 13, 14, 29, and 30 depend from claim 11 and are allowable for at least the reasons given above for claim 11.

Claims 2, 4, 6, and 8-10 depend variously from claim 1 and are allowable for at least the reasons given above for claim 1. Nothing in Inagawa cures the deficiencies in Aoki, Ridley, and Tottori noted above. In particular, nothing in Inagawa discloses or suggests both forming an interlayer over the conductive film, and that the annealing of the substrate is performed prior to forming the interlayer, as recited in claim 1.

Furthermore, nothing in Inagawa provides any reason that one skilled in the art would want to combine the teachings of Ridley or Tottori with those of Aoki as suggested by the Examiner.

Applicant therefore respectfully requests that the Examiner withdraw the rejection of claims 2, 4, 6, 8-11, 13, and 14 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Aoki, Ridley, and Tottori, and further in view of Inagawa.

The Examiner has rejected claim 15 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Aoki, Ridley, Tottori, and Inagawa, and further in view of United States Patent No. 6,159,781 to Pan et al. ("Pan").

Claim 15 depends from claim 11 and is allowable for at least the reasons given above for claim 11. Nothing in Pan cures the deficiencies in Aoki, Ridley, Tottori, and Inagawa noted above. In particular, nothing in Inagawa discloses or suggests that annealing is performed prior to performing the thermal diffusion process, as recited in claim 11.

Furthermore, Applicant notes that in this rejection, the Examiner is combining the teachings of five different references in order to obtain all of the limitations recited in claim 15. Applicant asserts that the Examiner is engaging in impermissible hindsight analysis, using the Applicant's own teachings to provide the reason to combine all of the individual elements of the recited claims. Nothing in any of Aoki, Ridley, Tottori, Inagawa, and Pan provide any reason why one of skill on the art would wish to combine all of their teachings in the particular manner suggested by the Examiner.

Applicant therefore respectfully requests that the Examiner withdraw the rejection of claim 15 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Aoki, Ridley, Tottori, and Inagawa, and further in view of Pan.

The Examiner has rejected claim 12 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Aoki, Ridley, Tottori, and Inagawa, and further in view of United States Patent No. 6,218,866 to Poplevine ("Poplevine").

Claim 12 depends from claim 11 and is allowable for at least the reasons given above for claim 11.

Nothing in Poplevine cures the deficiencies in Aoki, Ridley, Tottori, and Inagawa noted above. In particular, nothing in Poplevine discloses or suggests that annealing is performed prior to performing the thermal diffusion process, as recited in claim 11.

Furthermore, Applicant notes that in this rejection, the Examiner is combining the teachings of five different references in order to obtain all of the limitations recited in claim 12. Applicant asserts that the Examiner is engaging in impermissible hindsight analysis, using the Applicant's own teachings to provide the reason to combine all of the individual elements of the recited claims. Nothing in any of Aoki, Ridley, Tottori, Inagawa, and Poplevine provide any reason why one of skill on the art would wish to combine all of their teachings in the particular manner suggested by the Examiner.

Applicant therefore respectfully requests that the Examiner withdraw the rejection of claim 12 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Aoki, Ridley, Tottori, and Inagawa, and further in view of Poplevine.

The Examiner has rejected claim 16 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Aoki, Ridley, Tottori, and Inagawa, and further in view of United States Patent No. 6,218,300 to Narwankar et al. ("Narwankar").

Claim 16 depends from claim 11 and is allowable for at least the reasons given above for claim 11.

Nothing in Narwankar cures the deficiencies in Aoki, Ridley, Tottori, and Inagawa noted above. In particular, nothing in Narwankar discloses or suggests both forming an interlayer over the conductive film, and that the annealing of the substrate is performed prior to forming the interlayer, as recited in claim 1, and that annealing is performed prior to performing the thermal diffusion process, as recited in claims 1 and 11.

Furthermore, Applicant notes that in this rejection, the Examiner is combining the teachings of five different references in order to obtain all of the limitations recited in claim 16. Applicant asserts that the Examiner is engaging in impermissible hindsight analysis, using the Applicant's own teachings to provide the reason to combine all of the individual elements of the recited claims. Nothing in any of Aoki, Ridley, Tottori, Inagawa, and Narwankar provide any reason why one of skill on the art would wish to combine all of their teachings in the particular manner suggested by the Examiner.

Applicant therefore respectfully requests that the Examiner withdraw the rejection of claim 16 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Aoki, Ridley, Tottori, and Inagawa, and further in view of Narwankar.

The Examiner has rejected claim 28 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Aoki, Ridley, and Tottori, and further in view of United States Published Patent Application No. 2002/0052119 to Van Cleemput ("Van Cleemput").

Claim 28 depends ultimately from claim 1 and is allowable for at least the reasons given above for claim 1.

Nothing in Van Cleemput cures the deficiencies in Aoki, Ridley, and Tottori noted above. In particular, nothing in Van Cleemput discloses or suggests both forming an interlayer over the conductive film, and that the annealing of the substrate is performed prior to forming the interlayer, as recited in claim 1. Furthermore, nothing in any of Aoki, Ridley, Tottori, and Van Cleemput provide any reason why one of skill on the art would wish to combine all of their teachings in the particular manner suggested by the Examiner.

Applicant therefore respectfully requests that the Examiner withdraw the rejection of claim 28 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Aoki, Ridley, and Tottori, and further in view of Van Cleemput.

The Examiner has rejected claim 31 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Aoki, Ridley, Tottori, and Inagawa, and further in view of Van Cleemput.

Claim 31 depends ultimately from claim 11 and is allowable for at least the reasons given above for claim 11.

Nothing in Van Cleemput cures the deficiencies in Aoki, Ridley, Tottori, and Inagawa noted above. In particular, nothing in Van Cleemput discloses or suggests that that annealing is performed prior to performing the thermal diffusion process, as recited in claim 11.

Furthermore, Applicant notes that in this rejection, the Examiner is combining the teachings of five different references in order to obtain all of the limitations recited in claim 31. Applicant asserts that the Examiner is engaging in impermissible hindsight analysis, using the Applicant's own teachings to provide the reason to combine all of the individual elements of the recited claims. Nothing in any of Aoki, Ridley, Tottori, Inagawa, and Van Cleemput provide any reason why one of skill on the art would wish to combine all of their teachings in the particular manner suggested by the Examiner.

Applicant therefore respectfully requests that the Examiner withdraw the rejection of claim 16 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Aoki, Ridley, Tottori, and Inagawa, and further in view of Van Cleemput.

New Claims

By this response, Applicant has added new claims 32-43. No new matter has been added in these new claims. Applicant respectfully requests that the Examiner enter and consider these new claims.

Conclusion

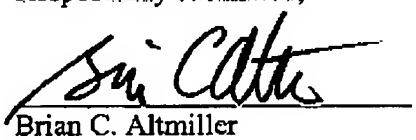
Applicant respectfully submits that, as described above, the cited prior art does not show or suggest the combination of features recited in the claims. Applicant does not concede that the cited prior art shows any of the elements recited in the claims. However, applicant has provided specific examples of elements in the claims that are clearly not present in the cited prior art.

Applicant strongly emphasizes that one reviewing the prosecution history should not interpret any of the examples Applicant has described herein in connection with distinguishing over the prior art as limiting to those specific features in isolation. Rather, for the sake of simplicity, Applicant has provided examples of why the claims described above are distinguishable over the cited prior art.

In view of the foregoing, Applicant submits that this application is in condition for allowance. A timely notice to that effect is respectfully requested. If questions relating to patentability remain, the Examiner is invited to contact the undersigned by telephone.

Although it is not anticipated that any additional fees are due or payable, the Commissioner is hereby authorized to charge any fees that may be required to Deposit Account No. 50-1147.

Respectfully submitted,



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